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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,673	11/24/2003	Wangguo Qin	188122002200	5631

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EXAMINER	
KIK, PHALLAKA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/721,673	QIN ET AL.	
	Examiner	Art Unit	
	Phallaka Kik	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/24/2003, 6/21/2004, 5/19/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-70* is/are pending in the application.

4a) Of the above claim(s) *63-69* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29,32-59,62 and 70* is/are rejected.

7)☒ Claim(s) *30,31,60 and 61* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/21/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action responds to the Application filed on 11/24/2003, IDS filed on 6/21/2004 and response to restriction/election filed on 5/19/2006. Claims 1-70 are pending, wherein claims 63-69 are withdrawn from consideration as being directed to non-elected inventions with traverse.

Election/Restrictions

2. Applicant's election with traverse of Invention I, claims 1-62,70 in the reply filed on 5/19/2006 is acknowledged. The traversal is on the ground(s) that claim 1 of invention I and claim 63 of invention II have similar language; therefore, inventions I (claims 1-62,70) and II (claims 63-67) should be rejoined. This is not found persuasive because although there are similar claim language as pointed out by Applicant, there are also sufficient differences as previously indicated by the Examiner in which the inventions as claimed do not overlap in scope and are not obvious variants of each other and have different mode of operation, because the reducing of the circuit elements in a bottom-up fashion from the leaf nodes to the root of the tree-like topological approximation as claimed in invention II do not overlap in scope and is not an obvious variants of invention I, which includes producing the topological approximation as a minimum spanning tree and identifying one or more symmetric nodes in a top-down fashion from the single input tree structure (see claims 5 and 7), and would therefore operate differently from the reducing steps/means of invention I (see Office Action mailed on 4/19/2006).

The requirement is still deemed proper and is therefore made FINAL.

3. Claims 63-69 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected inventions with traverse, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 5/19/2006.

4. This application contains claims drawn to inventions nonelected with traverse in paper filed on 5/19/2006. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

5. Applicant is reminded that upon the cancellation of claims to non-elected inventions, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Oath/Declaration

6. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:

Non-initialed and/or non-dated alterations (i.e., post office address of Kong Jun) have been made to the oath or declaration. See 37 CFR 1.52(c).

7. An Application Data Sheet in compliance with 37 CFR 1.76 may also be used to correct this particular type of defects (see 37 CFR 1.76 (c)(1)).

Drawings

8. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated (see paragraph [0006] of Applicant's specification). See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

9. **Claims 1-62,70** are objected to because of the following informalities:

As per **claim 1**, "the steps" (line 3) should be --steps--; "the effect" (line 5) should be --an effect--; "the topological" (lines 5-6) should be --topological--; "the reduction" (line 7) should be --a reduction-- for proper antecedent basis.

As per **claims 2,4,6,7**, "the step" (line 1) should be --a step-- for proper antecedent basis.

As per **claims 2-7**, the claims are also objected to for incorporating the above errors into the respective claims by claim dependency.

As per **claim 8**, "the steps" (line 3) should be --steps--;

"the effect" (line 5) should be --an effect--; "the topological" (lines 5-6) should be --topological--; "the reduction" (line 8) should be --a reduction-- for proper antecedent basis.

As per **claims 9,12,17,18,20,22-25,29,32,33**, "the step" (line 1) should be --a step-- for proper antecedent basis.

As per **claim 10**, "the steps" (line 1) should be --steps-- for proper antecedent basis.

As per **claim 14**, "the step" (line 1) should be --a step-- for proper antecedent basis; "the value" (line 2) should be --a value-- for proper antecedent basis.

As per **claim 15**, "the step" (line 1) should be --a step-- for proper antecedent basis; "the variation" (lines 1-2) should be --a variation-- for proper antecedent basis.

As per **claim 19**, "the steps" (line 1) should be --steps--; "the effect" (line 2) should be --an effect--; "the coupling" (line 5) should be --coupling--; "the cross-coupling" (line 6) should be --cross-coupling-- for proper antecedent basis.

As per **claim 21**, "the steps of" (line 1) should be --steps of:--; "the effect" (line 3) should be --an effect--; "the connection" (line 3) should be --a connection-- for proper antecedent basis and for proper grammar.

As per **claim 26**, "the steps" (line 1) should be --steps--; "the difference" (line 4) should be --a difference--; "the number" (line 4) should be --a number-- for proper antecedent basis.

As per **claim 27**, "the step" (line 1) should be --a step-- for proper antecedent basis; "notes" (line 2) should be --nodes-- for proper spelling.

As per **claim 28**, "claim 24" (line 1) should be --claim 27-- to provide for proper antecedent basis for the "eliminating one or more of said candidate nodes" (line 2); "the step" (line 1) should be --a step-- for proper antecedent basis.

As per **claim 30**, "the step" (line 1) should be --a step--; "the ground" (line 5) should be --ground-- for proper antecedent basis.

As per **claim 31**, "the step" (line 1) should be --a step--; "the value" (both occurrences on line 2; line 4 and 5) should be --a value-- for proper antecedent basis.

As per **claims 9-38**, the claims are also objected to for incorporating the above errors into the respective claims by claim dependency.

As per **claim 39**, "the effect" (line 8) should be --an effect--; "the topological" (lines 8-9) should be --topological-- for proper antecedent basis.

As per **claim 40**, --codes-- should be inserted after "executing" (line 2) for greater clarification.

As per **claim 47**, "the variation" (lines 1-2) should be --a variation-- for proper antecedent basis.

As per **claim 39**, "the effect" (line 2) should be --an effect--; "the coupling" (line 5) should be --coupling--; "the cross-coupling" (line 7) should be --cross-coupling-- for proper antecedent basis.

As per **claim 51**, "or, " (line 2) should be --and-- to be similar to claim 28.

As per **claim 56**, "the effect" (line 2) should be --an effect--; "the difference" (line 4) should be --a difference--; "the number" (line 4) should be --a number-- for proper antecedent basis.

As per **claim 57**, "notes" (line 2) should be --nodes-- for proper spelling.

As per **claim 61**, "the value" (all occurrences in lines 2 and 3) should be --a value-- for proper antecedent basis.

As per **claims 40-61**, the claims are also objected to for incorporating the above errors into the respective claims by claim dependency.

As per **claim 62**, "the effect" (line 4) should be --an effect--; "the cross-coupling" (line 8) should be --cross-coupling--; "the corresponding" (line 9) should be --corresponding-- for proper antecedent basis.

As per **claim 70**, "the effect" (line 6) should be --an effect--; "the topological" (lines 6-7) should be --topological--; "the reduction" (line 8) should be --a reduction-- for proper antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the

United States and was published under Article 21(2) of such treaty in the English language.

11. **Claims 1-4,8-12,18-20,22-23,34-35,39-42,46,48-50,52-53,62,70** are rejected under 35 U.S.C. 102(e) as being anticipated by **McGaughy et al.** (US Patent No. 7,024,652).

The applied reference has a common assignee and inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As per **claims 1-4,8-9,12,18-20,34-35,39-42,46,48-50,62,70**, all of the elements of the claims are illustrated in Fig. 8A (see also col. 13, lines 1-57), wherein the identifying of one or more elements are part of the static isomorphic partitioning, RC reduction, flattening (see col. 13, lines 12-43) as well as the adaptive and isomorphic partitioning (see col. 13, lines 44-57) which includes grouping or clustering of resistors and capacitors forming c-blocks (i.e., nodes connected via coupling capacitors as defined in Applicant's specification, paragraph [0043]), wherein the analysis and generation of the reduced topology corresponds to at least the dynamic adaptive partitioning in which the effect (i.e., strength of the coupling or coupling effects) is evaluated and if satisfies the predefined standard (i.e., less than a predefined threshold level or the effect is negligible), the circuit elements are combined (i.e., the other matrix

for the circuit elements are eliminated) into a single matrix, thus reducing the topology of the first circuit or forming an approximation thereof (see col. 8, lines 15-50); wherein such processes are being recursively executed until no further reduction is possible as shown by the circular arrows in Fig. 8A; and wherein the computer system, executable program code, memory, processor, computer executable software code, computer readable medium are part of the computer system as further described in col. 11, line 65 to col. 12, line 59.

As per **claims 10-11**, all of the elements of claims 9 from which the claims depend, are discussed in the rejection of claim 9 above, wherein since the threshold value is predefined, it is within the scope of the invention that this predefined threshold value be more than one values or as specified by the user.

As per **claims 22-23,52-53**, all of the elements of claims 8,46, from which the respective claims depend, are discussed in the rejection of claims 8,46 above, wherein the identifying and merging of one or more circuit elements having similar input-output characteristics are also described in col. 16, lines 16-43.

12. **Claims 1-4,8-9,12,15-16,20-21,24-29,37,39,46-47,50-51,54-59,70** are rejected under 35 U.S.C. 102(b) as being anticipated by **Sheehan** ("TICER: Realizable Reduction of Extracted RC Circuits", 1999 IEEE/ACM International Conference on Computer-Aided Design, November 7-11, 1999, pp. 200-203).

As per **claims 1-4,8-9,12,24-25,39,46,54-55,70**, all of the elements of the claims are summarized in column 2, page 200, wherein the identified elements represented as nodes are analyzed for effects of topological and physical characteristics (i.e., time

constant effects) in which the circuit are reduced by eliminating from the RC network (having a plurality of circuit elements, i.e., nodes) quick and slow nodes, which do not significantly alters its behavior (i.e., the effects are negligible; or satisfies the predetermined standards when the time-constant is less than or greater than minimum and maximum time constants defining the frequency of interest; wherein the recursively repeating the steps are also part of the successively finding quick and slow nodes in the circuit and then eliminating them (see page 201, last paragraph) and wherein since this method is a CAD (computer-aided design) implemented method (i.e., IEEE Transactions on Computer-Aided Design--see abstract), the programmed computer system, the at least one memory, the program code and the at least one processor for executing the code, the computer executable software code, and the computer readable medium are inherently included as part of the CAD system, being necessary to implement the CAD implemented method.

As per **claims 15-16,47**, all of the elements of claims 8,46, from which the respective claims depend, are discussed previously, wherein analysis of the delay measurement including the Elmore delays are also discussed on page 202, first column, last paragraph to second column, first paragraph.

As per **claims 20-21,26-27,50-51,56-57**, all of the elements of claims 8,24,39,54, from which the respective claims depend, are discussed previously, wherein the identifying of circuit clusters or groupings, moving a connection of one or more circuit elements connected to one or more nodes within one or more clusters to one or more

said center nodes, eliminating of neighboring nodes based on the number of nodes are also discussed in the quick nodes and slow nodes elimination (see page 201).

As per **claims 28-29,37,58-59**, all of the elements of claims 24,54, from which the respective claims depend, are discussed in the rejections of claims 24,54 above, wherein it is within the scope of the invention of the divider voltage structured being identified and not eliminated since the node(s) identified for nodes elimination include voltage nodes connected in the RC network (thus forming voltage divider structure) and such nodes are not eliminated (see page 201, first column).

13. **Claims 1-4,8-12,20,32-34,38-42,46,50,70** are rejected under 35 U.S.C. 102(b) as being anticipated by **Pong et al.** ("A Parasitics Extraction and Network Reduction Algorithm for Analog VLSI", IEEE Transactions on Computer-Aided Design, Vol. 10, No. 2, February 1991, pp. 145-149).

As per **claims 1-4,8-9,12,20,34,39-42,46,50,70**, all of the elements of the claims are summarized in section IV (page 149), wherein the identifying of one or more elements or clusters of elements is part of step (e), and the analyzing and generating the second topology (i.e., the simplified network or topology which is an approximation of the extracted network or first topology which are includes resistors and capacitors--see Fig. 6), including recursively perform the reduction until no further reduction is possible corresponds to step (f), wherein the predefined standard corresponds to the error threshold, and wherein this generating of the second topology is generated or reduced only when the effect is negligible since when the error threshold is exceeded, the network reduction is not carried out (see page 147, last paragraph); and wherein

since this method is a CAD (computer-aided design) implemented method (i.e., IEEE Transactions on Computer-Aided Design--see reference citation above and section VI), the programmed computer system, the at least one memory, the program code and the at least one processor for executing the code, the computer executable software code, and the computer readable medium are inherently included as part of the CAD system, being necessary to implement the CAD implemented method.

As per **claims 10-11**, all of the elements of claim 9, from which the respective claims depend, are discussed in the rejection of claim 9 above, wherein the use of a second predefined standard which is more relaxed than the first standard, is part of the use of user defined error threshold (see section IV, step b) which is allowed to be relaxed as further discussed on page 148, second column.

As per **claims 32-33**, all of the elements of claim 12, from which the respective claims depend, are discussed in the rejection of claim 12 above, wherein the identification and merging of the symmetrical nodes are also discussed on page 147 (first column, last paragraph to second column, last paragraph) in which the symmetrical nodes of Fig. 6 are identified and merged into simplified nodes.

As per **claim 38**, all of the elements of claim 8, from which the claim depends, are discussed in the rejection of claim 8 above, wherein since the method applies to VLSI (very large scale integrated) circuits, the topology containing the RC network being more 100 nodes is within scope of the **Pong et al.**.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. **Claims 5-7,13-14,17,43-45** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Pong et al.** ("A Parasitics Extraction and Network Reduction Algorithm for Analog VLSI", IEEE Transactions on Computer-Aided Design, Vol. 10, No. 2, February 1991, pp. 145-149) in view of **Teig et al.** (U.S. Application Publication No. 2006/0010412).

As per **claims 5,13,43**, **Pong et al.** disclose all of the elements of claims 4,12,42, from which the respective claims depend, as discussed previously. However, **Pong et al.** failed to specifically produce the topological approximation being a minimum spanning tree (MST). **Teig et a.** teaches the use of minimum spanning tree for modeling connections of the net's elements through the shortest route and efficiently provides wirelength estimate (see paragraphs [0095]-[0098]). It would have been obvious to one of ordinary skilled in the art at the time of the invention to further incorporate the use of minimum spanning tree of **Teig et al.** into the method/system of **Pong et al.** because such incorporation would allows the RC network star connections of **Pong et al.** to be modeled for further placement such that the net's elements through the shortest route and efficiently provides wirelength estimate as taught by **Teig et al.**.

As per **claims 14,17,44-45**, **Pong et al.** in view of **Teig et al.** disclose all of the elements of claims 13,43 as discussed above, from which the respective claims depend, wherein **Pong et al.** further teaches the identifying and eliminating of one or more circuit elements for which the value of the element(s) is less than a threshold value (i.e., user defined threshold error) (see page 147, first column, last paragraph to second column, last paragraph, in which the symmetrical nodes of Fig. 6 are identified and merged/eliminated into simplified nodes), wherein it would have been further obvious to one of ordinary skilled in the art at the time of the invention to also include these steps of identifying and eliminating one or more circuit elements using the minimum spanning tree of **Teig et al.** in order to arrive at the reduced RC network of **Pong et al.** since such RC network can be modeled using the minimum spanning tree as discussed above.

As per **claims 6-7**, **Pong et al.** disclose all of the elements of claim 1, from which the claims depend, including the identifying and eliminating of one or more circuit elements for which the value of the element(s) is less than a threshold value (i.e., user defined threshold error) (see page 147, first column, last paragraph to second column, last paragraph, in which the symmetrical nodes of Fig. 6 are identified and merged/eliminated into simplified nodes). However, **Pong et al.** failed to particular teach that the use of the tree structure. **Teig et a.** teaches the use of minimum spanning tree for modeling connections of the net's elements through the shortest route and efficiently provides wirelength estimate (see paragraphs [0095]-[0098]. It would have been obvious to one of ordinary skilled in the art at the time of the invention to

further incorporate use of minimum spanning tree of **Teig et al.** into the method/system of **Pong et al.** because such incorporation would allows the RC network star connections of **Pong et al.** to be modeled for further placement such that the net's elements through the shortest route and efficiently provides wirelength estimate as taught by **Teig et al.**.

16. **Claims 15-16,47** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Pong et al.** ("A Parasitics Extraction and Network Reduction Algorithm for Analog VLSI", IEEE Transactions on Computer-Aided Design, Vol. 10, No. 2, February 1991, pp. 145-149) in view of **Aji et al.** (US Patent Application Publication No. 2004/0044979).

As per **claims 15-16,47**, **Pong et al.** disclose all of the elements of claims 8 and 46, from which the respective claims depend, as discussed previously, but particular failed to make use of the RC values for analyzing the variation of one or more delay measurements, including Elmore delays. **Aji et al.** teach the analysis of the variation of the delay measurements using Elmore tree delay model based on the RC values extracted to provide optimal or near optimal solutions (see paragraphs [0083]-[0090]. It would have been obvious to one or ordinary skilled in the art at the time of the invention to further incorporate the delay analysis of **Aji et al.** into the system/method of **Pong et al.** because such incorporation would further make use of the RC values approximated by the method/system of **Pong et al.** to provide for optimal or near optimal delay analysis as further taught by **Aji et al.**.

17. **Claims 18-19,35-36,48-49,62** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Pong et al.** ("A Parasitics Extraction and Network Reduction

Algorithm for Analog VLSI", IEEE Transactions on Computer-Aided Design, Vol. 10, No. 2, February 1991, pp. 145-149) in view of **Muddu et al.** (US Patent No. 6,353,917).

As per **claims 18-19,35,48-49,62**, **Pong et al.** disclose all of the elements of claims 8,46, from which the respective claims depend, as discussed previously, including for preventing undesirable cross-talks (i.e., cross-coupling) (page 145, first paragraph under introduction section). However, **Pong et al.** failed to particular teach the identifying of the one or more circuit elements (including c-blocks which is defined as nodes connected via coupling capacitors--see Applicant's specification, paragraph [0043]) having coupling effects, including generating a second regional topology replacing the cross-coupling of each of the crossly-coupled node with its estimated coupling effects. **Muddu et al.** teach the analysis of coupling effects for the RC network, by identifying the one or more circuits elements having the coupling effects and replacing the RC network (i.e., for the crossly-coupled node(s)) with the lump model (i.e., estimated coupling effects) (see col. 10, line 30 to col. 11, line 48) that provides for greater accuracy (col. 2, lines 3-20). It would have been obvious to one of ordinary skilled in the art at the time of the invention to further incorporate the coupling effects analysis of **Muddu et al.** into the system/method of **Pong et al**. because such incorporation would further allow cross-coupling (i.e., cross-talk) to be analyzed while benefiting from the benefiting from the higher accuracy of **Muddu et al**.

Allowable Subject Matter

18. **Claims 30-31,60-61** are objected to due to the informalities set forth in this Office Action and as being dependent upon a rejected base claim, but would be allowable if

rewritten to overcome the noted informalities and if claims 30 and 60 are rewritten in independent form including all of the limitations of the base claim and any intervening claims.

19. The following is a statement of reasons for the indication of allowable subject matter:

As per **claims 30-31,60-61**, claims 30 and 60, from which the respective claims depend, recite the inventive steps/means for identifying a regional topology comprising two nodes N1 and N2 connected to a common node Na, wherein N1 is connected to Na through a resistance R1, N2 is connected to Na through resistance R2, N1 and N2 further having capacitance C1 and C2, respectively, connected either to the ground or another common node, and wherein there is no other resistor connection to N1 or N2, as claimed, as part of method/system of transforming a circuit from a first topology to a reduced topology, as claimed, which the prior arts made of record failed to teach or suggest. Accordingly, the claimed invention is novel and un-obvious over the prior arts made of record.

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Therefore, Applicant is requested herein to consider them carefully in response to this Office Action.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 571-272-1895. The examiner can normally be reached on Monday-Thursday, 8:30AM-7PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any response to this action should be mailed to:

Commissioner for Patents

P. O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

571-273-8300

Phallaka Kik
U.S. Patent Examiner
Art Unit 2825
August 16, 2006